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10/040,709	01/07/2002	William B. Gist	SMQ-044/P5286	2567

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EXAMINER	
OSBORNE, LUKE R	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,709	GIST ET AL.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 1-22 have been presented for reconsideration. No claims have been added or cancelled. Claims 1-22 are now pending in the instant application.

2. Applicants' arguments submitted 10/20/05 have been fully considered, Examiners response is as follows.

Claim Objections

3. Examiner acknowledges the amendment to Claim 10. Consequently the objection is withdrawn.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-6, 10-15, 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,933,356 to Rostoker et al, hereafter "Rostoker".

Regarding claim 1, Rostoker discloses in an electronic device, a method. See Figures 2, 4, 17, and the corresponding portions of Rostoker's specification for this disclosure. In Particular Rostoker teaches "In an electronic device, a method, comprising the steps of:

– providing simulation output from a simulation of an electrical component, said simulation output containing information regarding a data signal and a clock signal [Step 16 is Timing Simulation, Verification and Analysis (Column 21, lines 1-13)];

– providing an automated tool [Automated Design: Summary (Column 29, line 50 – Column 30, line 17)] for analyzing the information in the simulation output regarding the data signal and the clock signal and for producing a report of results of the analysis;

– receiving user-specified parameters at the tool [Optimization is then performed according to user-defined timing constraints (see User Interface; FIG. 20) and those dictated by existing blocks. This is an iterative process. Constraints need to be refined until the desired timing and area requirements are achieved (Column 22, lines 38 - 42)]; and

– applying the user-specified parameters to configure the analysis performed by the tool [Optimization is then performed according to user-defined timing constraints (see User Interface; FIG. 20) and those dictated by existing blocks. This is an iterative process. Constraints need to be refined until the desired timing and area requirements are achieved (Column 22, lines 38 - 42)]; and

– performing the analysis of the simulation output with the tool to produce the report of the analysis [The logic simulator takes the schematic object file(s) and simulation models, and generates a set of simulation results, acting on

instructions initial conditions and input signal values provided to it either in the form of a file or user input]

[In the present invention, a series of programs are run which invoke, operate on the data from, and integrate the capabilities of a number of existing design tools (simulators, data analysis, etc.). These programs operate on the logic schematic data base prepared by the user, prepare input files for the existing tools, invoke the existing tools, analyze the output files thereof, and ultimately combine the outputs of the existing tools into useful logic models (Column 6, lines 60-67)]" as claimed.

Applicants Arguments

Rostoker fails to disclose each and every element of claim 1. The citations Examiner has indicated does not disclose each and every limitation in the claim as recited.

Examiners Response

In the present invention, a series of programs are run which invoke, operate on the data from, and integrate the capabilities of a number of existing design tools (simulators, data analysis, etc.). These programs operate on the logic schematic data base prepared by the user, prepare input files for the existing tools, invoke the existing tools, analyze the output files thereof, and ultimately combine the outputs of the existing tools into useful logic models. The end result is the appearance to the user of an automatic process of logic model generation. This process of input file preparation and output file analysis would ordinarily be performed by human operators, often by many different people due to the different skill levels required at each step [Column 6, line 60 – Column 7, line 5)] This automatic data analysis includes timing analysis. In order to verify the timing accuracy of the model, a verification step is performed whereby the input stimuli used for the circuit-level simulation are converted to a format usable by the

logic-level simulator and are applied to the newly created logic model. The resultant outputs from the logic-level simulator are compared with the outputs from the circuit-level simulator, and if the output transitions from the two simulations do not deviate by more than some pre-determined amount, then the logic model is said to be accurate and is ready for use [Column 8, lines 56-67]. The arguments directed toward the other claims are traversed for similar reasons.

Regarding claim 2, Rostoker discloses the method of claim 1 "further comprising the step of performing error checking on the simulation output to identify any errors in the simulation output [Optimization is then performed according to user-defined timing constraints (see User Interface; FIG. 20) and those dictated by existing blocks. This is an iterative process. Constraints need to be refined until the desired timing and area requirements are achieved (Column 22, lines 38 - 42)]" as claimed.

Regarding claim 3, Rostoker discloses the method of claim 1 "wherein the report contains information regarding hold times of the data signal [Timing constraints may include the following: maximum and minimum rise/fall delay, set-up and hold check, length of clock cycle and maximum transition time per net. The timing constraints may also include boundary conditions, such as signal skew at the module's inputs, drive capabilities of the modules outputs, etc., when such data is available (Column 20, lines 31-37)]" as claimed.

Regarding claim 4, Rostoker discloses the method of claim 1 "wherein the report contains information regarding setup times of the data signal [Timing constraints may include the following: maximum and minimum rise/fall delay, set-up and hold check, length of clock cycle and maximum transition time per net. The timing constraints may also include boundary conditions, such as signal skew at the module's inputs, drive capabilities of the modules outputs, etc., when such data is available (Column 20, lines 31-37)]" as claimed.

Regarding claim 5, Rostoker discloses the method of claim 1 "wherein the report contains information regarding data jitter [Timing constraints may include the following: maximum and minimum rise/fall delay, set-up and hold check, length of clock cycle and maximum transition time per net. The timing constraints may also include boundary conditions, such as signal skew at the module's inputs, drive capabilities of the modules outputs, etc., when such data is available (Column 20, lines 31-37)]" as claimed.

Regarding claim 6, Rostoker discloses the method of claim 1 "wherein the simulation output contains information regarding the data signal and the clock signal for a simulated time period and wherein the user-specified parameters include a specification of a portion of the simulated time period to which the analysis is to be applied

> [Step 11 deals with Timing/Area Constraints. These are used to customize the optimization process. Optimization is usually driven by area and speed (timing constraints. These might instruct the tool to perform rudimentary area versus speed trade off on individual or small clusters of gates, or to perform comprehensive area and speed optimizations in combination with other constraints such as drive capability. A rich set of constraint constructs is required for meaningful

design optimization, and are provided in the methodology of this invention (Column 20, lines 22-31)]" as claimed.

Claims 10-15 contain the same limitations regarding the computer program product as method claims 1-6, thus are rejected for the same reasons as claims 1-6.

Claim 19 contains the same limitations as claim 5, thus is rejected for the same reasons as claim 5

Claim 20 contains the same limitations as claim 1, thus is rejected for the same reasons as claim 1.

Regarding claim 21, Rostoker discloses the method of claim 19, "wherein the step of processing the results processes the results for only a portion of the simulated time period [This leads to unit clauses which give the final resolved values of every signal present in the design description, in the simulation results 2210 (Column 28, lines 56- 59)]" as claimed.

Claim 22 contains the storage medium limitations similar to the method limitations of claim 19, thus is rejected for the same reasons as claim 22.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 7, 8, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of Nourani, Mehradad et al, "Built-In Self-Test for Signal Integrity" June 18, 2001 pages 792-797 hereafter, "Nourani".

Regarding claim 7, Rostoker teaches the method of claim 1 as discussed *supra* and has a user interface [Figure 20] for the input of user configuration parameters.

Rostoker does not expressly teach wherein the user-specified parameters include a specification of a voltage reference window extending from a logically high reference voltage to a logically low reference voltage as claimed.

Nourani teaches the signal integrity model as disclosed. Nourani teaches as shown in Figure 2 the variable window and the associated errors that can occur.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the signal integrity model as taught by Nourani with the simulation method of Rostoker.

The motivation for doing so would have been as Nourani teaches to incorporate a practical view of integrity loss into the device modeling [Page 793, Section 3.2 A model for Signal Integrity].

Claim 16 contains the same limitation as claim 7, thus is rejected for the same reasons as claim 7.

Regarding claim 8, Rostoker teaches the method of claim 1, wherein signals are used.

Rostoker does not expressly teach that the signals are single ended.

Nourani teaches signal integrity of single ended signals as shown in Figure 2.

At the time of invention it would have been obvious to a person of ordinary skill in the art to use single ended signals as taught by Nourani, with the simulation method of Rostoker.

The motivation for doing so would have been to use common digital logic as shown in Rostoker Figure 12.

Claim 17 contains similar limitations as claim 8 thus is rejected for the same reasons as claim 8.

7. Claims 9, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker in view of "Inside differential signals" by Cadence, 2001, retrieved from www.winnet.com.cn/Cadence/High_Speed_Design/ Inside_Differential_Signals.pdf 4 pages hereafter "Cadence".

Regarding claim 9 Rostoker teaches the method of claim 1, wherein signals are used.

Rostoker does not expressly teach that the signals used are differential as claimed.

Cadence teaches the use of differential signals, page 1, Why use differential signals.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use differential signals as taught by Cadence with the simulation method taught by Rostoker.

The motivation for doing so would have been to use lower voltage swings, resulting in faster circuits, and reduced electromagnetic interference. Page 1 why use differential signals.

Claim 18 contains the same limitations as claim 9, thus is rejected for the same reasons as claim 9.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LRO

Paul L. Rodriguez 1/9/06

Primary Examiner
Art Unit 2125